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SF-7735

B. E. - IV (Sem. VIII) (ELectronics & Communication) Examination

May / June - 2011

VLSI Circuits

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ B. E. - 4 (SEM. 8) (ELECTRONICS & COMMUNICATION)

Name of the Subject :

☛ VLSI CIRCUITS

☛ Subject Code No. : 7 7 3 5 ☛ Section No. (1, 2,.....) : NIL

Seat No. :

Student's Signature

(2) Attempt all questions.
(3) Figures to the right indicate full marks.
(4) Make suitable assumption if required.

1 (a) Answer the following questions (Two marks each) **14**

(i) Why W/L ratio of PMOS is more than W/L ratio of NMOS transistor for CMOS gates ?

(ii) Draw circuit of Tri state buffer using CMOS gate.

(iii) Compare π model with T model of Interconnect.

(iv) Name any two companies in India which work in area of VLSI circuits design.

(v) Explain race condition.

(vi) Explain Cross talk in Interconnect.

(vii) Let oscillation frequency of a ring oscillator is 200 MHz. Consider delay of an inverter τ = 50ps. Identify number of stages in ring oscillator.

(b) Fill in the Blanks (One mark each) **6**

(i) In CMOS logic gate if pull down network is connected in series then pull up network is connected in _____.

(ii) If width of transistor increases, resistor of transistor _____.

(iii) Let Vg is gate voltage = V_{DD} and Vs is source voltage = V_{DD} then, maximum output voltage of NMOS pass transistor is _____.

(iv) QFP package is known as _____package.

(v) In NMOS transistor current flows from _____ after channel formation.

(vi) Distance between drain to source is _____ in 300 nm process.

2 (a) Sketch $Y=\overline{(A+B+C)}\cdot D$ with transistor widths chosen to achieve equal effective rise and fall resistance. Also sketch RC delay model for same. **7**

(b) Explain types of photoresists and their usage in lithography process with appropriate diagram. **8**

OR

2 (a) Explain D Latch with appropriate diagram and waveforms. **3**

(b) Discuss drive strength of pass transistor and transmission gate. **4**

(c) Two-input NOR gate drives : **8**

(i) 4 identical NOR gates

(ii) 4 identical NAND gates

Calculate delay in the driving NOR gate for both cases and illustrate in which case delay will be more.

3 Attempt any three of the following : **15**

(i) Explain dynamic NAND gate with diagram.

(ii) Discuss carry chain method of addition.

(iii) Discuss package options of IC and chip to package connection.

(iv) Write short note on cross talk and its implications.

(v) Explain skew gates.

4 Answer the following questions (Two marks each) **20**

(i) Explain case statement.

(ii) Explain the difference between with .....select and when..... else statement

(iii) Signal X : std_logic_vector (3 down to 0) : = "1011";
Signal Y : std_logic_vector (0 to 3): = : "1011";
A <= not X;
B <= Y
What will be value of B(3), B(2), B(1), B(0), A(3), A(2), A(1), A(0) ?

(iv) Explain FOR loop with example.

(v) What is component instantiation ?

(vi) State difference between signal and variable.

(vii) Declare an enumerated data type called VOWEL containing only vowel characters.

(viii) If you want to use tri-state logic, which data type and package you will use ?

(ix) State importance of wait statement.

(x) Compare CPLD with FPGA.

5 Attempt any three of the following : **15**

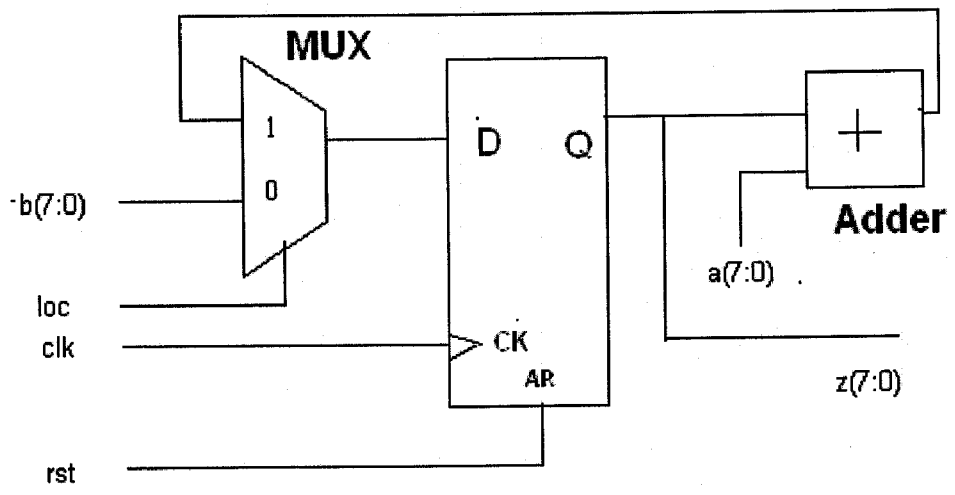
(i) Explain next statement in VHDL with an example.

(ii) Write VHDL code for 1x4 de-multiplexer using if.....else statement.

(iii) Write VHDL code for 4 bit ripple adder using equations.

(iv) Write VHDL code for serial in parallel out shift register.

(v) Write behavioural VHDL code for the circuit shown in figure below.



6 Attempt any three of the following : **15**

(i) Write short notes on delays in VHDL.

(ii) Compare PAL, PLA and PLD with appropriate diagram.

(iii) Differentiate between Standard cell based ASIC and Gate array based ASIC design methods.

(iv) Discuss architecture of FPGA using block diagram.

(v) With diagram compare FUSE and ANTIFUSE mechanism of programming FPGA.
